UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company, Plaintiff, v. MITAC COMPUTING TECHNOLOGY CORPORATION and MITAC HOLDINGS CORPORATION, a Taiwan corporation, Defendants. ASUSTEK COMPUTER, INC., Defendant. INVENTEC CORPORATION, a Taiwan corporation, Defendant. LENOVO GROUP Ltd. et al., Defendants. WIWYNN CORPORATION, a Taiwan corporation, Defendants.	***CONSOLIDATED*** **JURY TRIAL DEMANDED** Civil Action No.: 6:20-cv-962-ADA Civil Action No.: 6:20-cv-965-ADA Civil Action No.: 6:20-cv-966-ADA Civil Action No.: 6:20-cv-967-ADA Civil Action No.: 6:20-cv-968-ADA

ACQIS'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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3	U.S. Patent No. 8,977,797 ("'797 patent")
4	U.S. Patent No. 7,676,624 ("'624 patent")
5	U.S. Patent No. 8,041,873 ("'873 patent")
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I. INTRODUCTION

The ACQIS inventions address two primary goals: (1) improving the performance of computer communications with a new physical interface channel to replace existing buses like PCI or USB, while (2) maintaining software compatibility with systems using all types of PCI or USB communications. To those ends, the ACQIS patents claim a new physical interface channel—not prior art PCI or USB buses—that continues to communicate certain PCI or USB information, like "address bits" or "data bits," thereby maintaining software compatibility. The claimed inventions specify *what* PCI or USB information is communicated while improving *how* it is communicated. ACQIS has proposed constructions consistent with the framework in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) that identify the information claimed to communicate through this improved communication channel.

Defendants' constructions, in contrast, do not specifically address what PCI or USB information must be transmitted. As a result, they propose a construction that does not take into account the claim language or the specification, attempting to improperly limit all claims, irrespective of the claim language, to require every element of the PCI Specification or USB 2.0 Specification in their entireties. This would exclude preferred embodiments, contradict the claims, and perversely limit the invention to the very prior art products the invention intends to replace. Defendants also seek constructions improperly limited to specific forms of computers, like blade servers, and particular chip types not reflected in the claims or supported by intrinsic or extrinsic evidence to advance their non-infringement positions.

ACQIS proposes constructions that resolve key disputes now, comport with the patent claims and specifications as well as statements before the patent office, include relevant embodiments, and comport with the *Phillips* framework. The Court should adopt ACQIS's constructions.

II. BACKGROUND

A. ACQIS's Inventions

Dr. William Chu, the inventor of the ACQIS patents, made communications between computer components faster, more efficient, and less costly. He invented a new computer communication interface channel to replace the burdensome physical and electrical requirements of prior art computer buses such as the parallel Peripheral Component Interconnect (PCI) bus or the Universal Serial Bus (USB). Ex. 1, '768 patent at 3:23-4:16, 5:47-49, 25:13-16. His inventions make communication between computer components faster, more reliable, and more power-efficient while also reducing the number of wires and "pins" (electrical connections) needed. At the same time, Dr. Chu's new interface channel can still communicate certain information specified by prior industry specifications, such as PCI or USB, to maintain software compatibility with prior and existing systems using newer versions of PCI and USB technology.

In short, Dr. Chu's inventions enable systems to preserve *what* information is communicated—such as address, data, or byte enable information—while improving *how* it is communicated—using Dr. Chu's improved physical channel design. ACQIS's licensees and Defendants have used Dr. Chu's inventions in computers and servers for years to enable faster, smaller devices with better battery life.

Before Dr. Chu's inventions, prior art PCI buses used a "parallel" interface to transfer data between components. *Id.* at 3:23-4:16. These buses transferred multiple bits together—in "parallel"—represented by electrical signals on a high-voltage, parallel array of wires connecting two devices. Ex. 16, Levitt Decl. ¶¶ 40-43. Parallel buses suffered from limitations on communication speeds and high voltage requirements. *Id.*

Dr. Chu's invention replaces prior art parallel wires and corresponding control signals

used to manage the parallel transmissions with an interface that communicates information serially—one bit at a time over each electrical line in the interface. Ex. 1, '768 patent at 6:41-52; Ex. 16, Levitt Decl. ¶ 44. His inventions replaced the parallel PCI interface, which had approximately 50 parallel wires to carry 32 bits of address and data information, with a serial interface using much fewer wires. *Compare* Ex. 1, '768 at Fig. 16 (describing the signals transmitted using a prior art parallel PCI bus) *with id.* at Fig. 13 (showing invention embodiment with fewer signal lines); Ex. 16, Levitt Decl. ¶¶ 45-46. This allowed the use of Low Voltage Differential Signal ("LVDS") channels, which transmit information faster and with less power consumption than PCI and other buses. Ex. 1, '768 patent at 5:47-6:11. Reducing the number of wires also reduces the pins required on the devices to connect to such wires and accordingly reduces size and cost. *Id.* at 6:3-11.

Dr. Chu's new interface channel is versatile. Some embodiments of Dr. Chu's invention replace the "bridge" interface between two devices that each have their own parallel PCI bus. *See, e.g.*, *id.* at Fig. 10. Other embodiments apply Dr. Chu's improved serial interface to direct connections between devices without PCI buses, obviating any need for a parallel bus. *See id.* at Figs. 8A and 8B.

Dr. Chu's many inventions stem from his unique modular computer system (like what is shown in Figure 1 of the '768 patent). ACQIS received patent protection over many aspects of the modular computer system. This case and the claims at issue focus on one aspect of the system: the new computer communication interface channel used in the system. Dr. Chu's inventions are used in a variety of applications. For example, earlier cases focused on emerging blade server technology—*e.g.*, computer chasses or enclosures for housing multiple blade modules. Ex. 16, Levitt Decl. at ¶ 149. Over time, use of the claimed serial PCI interface channel

continued to spread and ultimately became fundamental to almost all computer systems—including personal computers, servers, smartphones, and games consoles—not just blade servers. *See, e.g.*, Lenovo Complaint[1] ¶¶ 36-39. The patents and claims at issue in this case directly apply to the broader computer and server markets. Ex. 16, Levitt Decl. at ¶ 149. Not only has the serial PCI interface claimed been widely adopted, but the computer industry also adopted a USB standard known as USB 3.0, which also uses the LVDS serial interface technology Dr. Chu invented. Put simply, Dr. Chu's invention was foundational to two industry standards—PCI Express (i.e., a form of serial PCI) and USB 3.0—that have become ubiquitous.

Dr. Chu filed the utility applications leading to his patents in 1999 and 2000, and the '768, '750, and '797 patents claim priority to a provisional application filed in 1999. Claim construction in this matter thus must consider what meaning the terms at issue would have had to a person of skill in the art in this time period. *Phillips*, 415 F.3d at 1313.

B. Procedural Background

ACQIS has asserted 15 patents in the six litigations captioned above, the '624, '873, '977, '359, '768, '769, '750, '984, '602, '468, '797, '654, '739, '140, and '947 patents. The asserted patents fall into three groups: (1) the '768, '750, '797, '359, '977, and '769 patents share largely identical written disclosures; (2) the '873 and '624 patents share largely identical written disclosures that substantially overlap with the disclosures of the first group[2]; and (3) the '654, '140, '602, '984, '468, '739, and '947 patents share identical written disclosures. Additionally, the disclosures of the last group of patents overlap substantially overlaps with the first two

[1] *ACQIS LLC v. Lenovo Group Ltd., et al.,* No. 6:20-cv-00967, Dkt. 1 (W.D. Tex. Oct. 15, 2020).
[2] The substantive differences between the first group and second group of asserted patents are that the first group has additional figures (i.e., Figures 8A-C and 24-31) and text in the specification discussing the additional figures. *See, e.g.*, Ex. 1, '768 patent at 16:27-36, 22:64-24:32, 25:8-12, 38:43-45, and 40:23-34.

groups.[3] Defendants do not appear to dispute the substantial overlap. *See* Dkt. 77 at 2. For simplicity, in this brief ACQIS primarily cites the '768 patent's specification unless meaningful differences exist with the other patents.

Judge Davis of the Eastern District of Texas and Judge Burroughs of the District of Massachusetts previously have construed terms from other ACQIS patents not at issue here. *ACQIS LLC v. Appro Int'l, Inc.*, No. 6:09-CV-148, 2011 U.S. Dist. LEXIS 10515 (E.D. Tex. Feb. 3, 2011) ("*Appro*"); *ACQIS LLC v. Alcatel-Lucent USA Inc.*, No. 6:13-CV-638, 2015 U.S. Dist. LEXIS 48339 (E.D. Tex. Apr. 13, 2015) ("*Alcatel-Lucent*"); *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2017 U.S. Dist. LEXIS 202160 (D. Mass. Dec. 8, 2017) ("*EMC I*"); *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2021 U.S. Dist. LEXIS 55945 (D. Mass. Feb. 19, 2021) ("*EMC II*"). Some of these terms included the same or similar language present in the claims here, such as "PCI bus transaction." None of the prior constructions, however, addressed the specific claim language or disclosures of the intrinsic record for the 15 patents at issue here.[4] In addition, Chief Magistrate Judge Payne of the Eastern District of Texas recently held a *Markman* hearing relating to five of the ACQIS patents at issue here, but he has not yet issued a claim construction order for that case. *ACQIS LLC v. Samsung Elec. Co., Ltd., et al.*, No. 2:20-cv-00295-JRG (E.D. Tex. Aug. 23, 2021) ("*Samsung*").

III. ARGUMENT

ACQIS's proposed constructions align with the inventions, as recited in the claims and

[3] For example, Figures 8A, 8B, 10, and 12 of the '768 patent correspond with Figures 19, 20, 14, and 23, respectively, of the '654 patent. Portions of the patents' specification are also substantially the same. For example, compare Ex. 1, '768 patent at 17:56-64, 18:63-19:17, and 25:3-7 to Ex. 12, '654 patent at 19:37-45, 19:48-54, and 20:66-21:3, respectively.

[4] For example, the *EMC* court did not address the phrases at issue here reciting "address and data bits of a Peripheral Component Interconnect (PCI) bus transaction" or "address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction." *See EMC II*, 2021 U.S. Dist. LEXIS 55945, at *5-6.

described in the specifications, and their improvements over prior art PCI and USB buses. ACQIS's constructions of the "PCI" terms incorporate the PCI-based information expressly recited in the claims and described in the specifications' embodiments of the invention, allowing software compatibility with traditional PCI devices while using the invention's improved LVDS interface channel. ACQIS's constructions for the "USB" terms likewise apply this framework of preserving software compatibility while implementing the improved channel.

Defendants' constructions, in contrast, appear to either (1) narrow the claim by importing compliance with every page of the PCI or USB specifications in existence at the time of the patents' priority applications, thus entirely contradicting the purpose of the inventions and excluding key embodiments, or (2) fail to provide meaningful specificity as to what exactly the specific claim terms do require. These constructions do not align with the intrinsic disclosures of the ACQIS patents or how a POSITA would understand the extrinsic evidence at the time of the invention. Moreover, Defendants fail to address particular differences in language between the claims, thus improperly rendering certain terms superfluous.

A. "Peripheral Component Interconnect (PCI) bus transaction" / "PCI bus transaction"

ACQIS's Construction	Defendants' Construction
Information, including at least PCI address, data, byte enable, and command type information, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component	A transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component

The parties' dispute about the "PCI" terms relate to which aspects of the PCI Local Bus Specification the claims address. The parties do not appear to dispute that, at the time of the ACQIS inventions, the term "PCI" referred to the "PCI Local Bus Specification" ("PCI

Specification"), including revisions of that Specification up to version 2.2. However, the parties disagree as to what aspects of the PCI Specification the claims require with respect to the phrase "PCI bus transaction."

The claims, specifications, and the PCI Specification itself explain that a "PCI bus transaction" in the ACQIS patents includes at least four types of PCI information: (1) address, (2) data, (3) byte enable, and (4) command information, as ACQIS has proposed. A "PCI bus transaction" when used alone in the claims requires these four types of information, but notably, some of the claims do not require ***all*** four types of information and expressly recite only certain bits of a "PCI bus transaction."[5] *See* Section III.B. While the Defendants unhelpfully seek to define "transaction" as "transaction," ACQIS's construction aligns with Judge Davis's prior construction—"information, in accordance with the PCI standard, for communication with an interconnected peripheral component"—while providing additional specificity that addresses a fundamental dispute between the parties. *Alcatel-Lucent*, 2015 U.S. Dist. LEXIS 48339, at *15. The construction of the claimed "PCI bus transaction" requires this additional specificity to resolve likely infringement disputes in this litigation. Because of a similar lack of specificity in the *EMC* court's construction, that court erroneously applied the "PCI bus transaction" term as if it required every element of the specification "in its entirety," even though it had been consistently construed to ***not*** require ***every*** aspect of the PCI Specification. The Court can avoid such problems in this litigation by adopting ACQIS's proposed construction.

Defendants' construction fails to specify which parts of the PCI Specification are required for a "PCI bus transaction" in accordance with the patent claims. Thus, their proposed

[5] Some claims specifically recite address bits, data bits, and byte enable information bits of a "PCI bus transaction" (Ex. 2, '750 patent at 40:39-43), while other claims recite just the address and data bits of a "PCI bus transaction." *Id.* at 41-37.

construction is so ambiguous that a person of ordinary skill in the art would be unable to determine whether "PCI bus transaction" requires all or only certain parts of the PCI Specification. At the same time, Defendants' construction is inconsistent with the intrinsic and extrinsic evidence and violates the canons of claim construction by improperly excluding disclosed embodiments.

1. The claims and specification show that a "PCI bus transaction" includes PCI address, data, and byte enable bits and command information.

The Claims: Since some of the claims recite an LVDS channel to convey specific subsets of bits of a "PCI bus transaction" in serial form, those claims can be used to helpfully identify some of the specific bits which must be part of a "PCI bus transaction." For example, claim 1 of the '750 patent recites the phrase:

> …a first Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial bit stream….

Ex. 2, '750 at 40:39-43. On its face, claim 1 of the '750 patent specifically requires only "address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction." Other claims, however, require different specific bits. For example, claim 5 of the '750 patent recites "address and data bits of a Peripheral Component Interconnect (PCI) bus transaction," but it does not recite "byte enable information bits." *Id.* at 41:3-7. The claims do not recite any information or bits required for a "PCI bus transaction" other than these three types. Thus, the claim language indicates that a "PCI bus transaction" includes address bits, data bits, and byte enable bits, which is consistent with ACQIS's proposed construction.[6] Defendants'

[6] As discussed in the following section ("The Specification"), the patent specification indicates that a "PCI bus transaction" also includes a fourth type of information—"command information."

accusation that ACQIS has "cherry-picked" the types of information required for a "PCI bus transaction" (Dkt. 77 at 9), is simply a recognition that the claim language makes that selection expressly to give each claim term meaning. *See Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so."; reversing district court claim construction); *Gen. Am. Transp. Corp. v. Cryo-Trans, Inc.*, 93 F.3d 766, 770 (Fed. Cir. 1996) (rejecting district court claim construction because it rendered claim term superfluous). Whether, in the abstract, a "PCI bus transaction" could refer to all aspects of the PCI Specification is not relevant, what matters here is the context of the claim language and the invention, which expressly limit the invention to transmitting only certain bits that are traditionally used in such a transaction. *See, e.g., Fenner Invs., Ltd. v. Cellco P'ship*, 778 F.3d 1320, 1322-23 (Fed. Cir. 2015) ("The terms used in patent claims are not construed in the abstract, but in the context in which the term was presented and used by the patentee[.]"). ACQIS's proposed construction stays true to the claim language; "PCI bus transaction" requires address bits, data bits, and byte enable information bits. *See also Phillips*, 415 F.3d at 1316 ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.") (internal citations omitted).

The Specification: The embodiments in the ACQIS specifications describe what information the invention includes in a "PCI bus transaction": the address bits, data bits, and byte enable information bits recited in the claims as well as an additional item, command information. The specifications describe an embodiment of the claimed LVDS channel as the "XPBus"—the invention's replacement for a traditional PCI bus or bridge. *See, e.g.*, Ex. 1, '768 patent at 21:23-36, Fig. 12 (describing LVDS signals for XPBus embodiment), 24:28-47, Fig. 31 (describing

"LVDS lines of XPBus"). The '768 patent, for example, illustrates the "XPBus" in Figures 6, 8A, 8B, 8C, 9, 10, 11, 28, 29, and 30; it explains that Figures 12, 13, and 14 describe information transferred over the XPBus in various embodiments; and it describes the LVDS lines of an XPBus embodiment in Figures 15 and 31. *Id.* at 8:40-52, 21:23-22:63, 24:28-52.

The '768 patent's specification contrasts the signals used with a traditional parallel PCI bus to the more limited and more efficient information transferred by the invention's new serial communication interface. Figure 13 describes information transferred over the XPBus LVDS channels of the invention. *Id.* at 21:37-22:4. Figure 16, in contrast, describes the signals transmitted using a prior art parallel PCI bus. *Id.* at 25:13-16.[7] The overlap and non-overlap between these figures—Figure 13 describing the invention, and Figure 16 the prior art—demonstrates which information from the PCI specification the invention includes in a "PCI bus transaction," and which parts it no longer needs by using its improved interface channel. The purpose of the invention is to provide an interface that is *compatible* with traditional PCI communications, not to provide an interface that is exactly like the prior art PCI Specification.

For example, Figure 13 shows that the invention's interface channel transmits four of the types of PCI information that appear in Figure 16: "PCI address A[31:00]" represented by A00 to A31, "PCI data D[31:00]" represented by D00 to D31, "PCI command information" represented by CM0# to CM3#, and "PCI byte enable information" represented by BE0# to BE3#. *Id.* at 21:37-58.

[7] Although the '984, '602, '468, '654, '739, '140, and '947 patents do not include Figures 13 and 16 and their corresponding description from the '768 patent, they describe the same structure of XPBus and do not suggest any different interpretation of a "PCI bus transaction." *See, e.g.*, Ex. 9, '984 patent at Fig. 16 (corresponding to the '768 patent's Fig. 15, which shows the same types of information as Fig. 13); Ex. 10, '602 patent at Fig. 16 (same); Ex. 11, '468 patent at Fig. 16 (same); Ex. 12, '654 patent at Fig. 16 (same); Ex. 13, '739 patent at Fig. 16 (same); Ex. 14, '140 patent at Fig. 16 (same); Ex. 15, '947 patent at Fig. 16 (same). Accordingly, ACQIS proposed construction of "PCI bus transaction" is consistent across the 15 asserted patents.

Chu Fig. 13, illustrating PCI address information, data information, byte enable information, and command information

PCK	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-	CK+	CK+	CK+	CK+	CK+	CK-	CK-	CK-	CK-	CK-
PD0	BS0	CM0#	A00	A01	A02	A03	A04	A05	A06	A07	BS0	BE0#	D00	D01	D02	D03	D04	D05	D06	D07
PD1	BS1	CM1#	A08	A09	A10	A11	A12	A13	A14	A15	BS1	BE1#	D08	D09	D10	D11	D12	D13	D14	D15
PD2	BS2	CM2#	A16	A17	A18	A19	A20	A21	A22	A23	BS2	BE2#	D16	D17	D18	D19	D20	D21	D22	D23
PD3	BS3	CM3#	A24	A25	A26	A27	A28	A29	A30	A31	BS3	BE3#	D24	D25	D26	D27	D28	D29	D30	D31
PCN	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9	CN0	CN1	CN2	CN3	CN4	CN5	CN6	CN7	CN8	CN9

FIGURE 13

Id. at Fig. 13 (color and title added); Ex. 16, Levitt Decl. ¶¶ 31-32, 84. PCI "bus command[s]" describe the type of operation, such as a read or write, and "Byte Enables" indicate the valid bytes of data. Ex. 16, Levitt Decl. ¶¶ 80-83. The information in Figure 13 overlaps with the specific bits of a PCI bus transaction recited in the claims: "address bits," "data bits," and, in certain claims, "byte enable information bits." Figure 13 does not include ***any*** of the other signals in Figure 16 used to control a parallel PCI bus, such as "PAR" ("Parity"), "FRAME#," "IRDY#," and "TRDY#." Ex. 1, '768 patent at Fig. 13, 21:37-22:4, Fig. 16. Instead, it replaces those signals with new bits, different from existing PCI (and thus not in Figure 16), to control transmission over the XPBus—as one would expect where the invention replaces and improves on the prior art parallel PCI bus. Ex. 16, Levitt Decl. ¶ 32. For example, Figure 13 describes bits "BS0 to BS3" that "represent 4 bits of bus status data indicating the status of the XPBus." Ex. 1, '768 patent at 21:40-47. Figure 13 also includes bits "CN0 to CN9," which "represent 10 bits of control information sent in each clock cycle." *Id.* In short, the claimed inventions are compatible with, but different from, prior art PCI communications that is defined by *all* of the PCI Specification.

The '768 patent's specification explains that the invention's bus status bits can represent "*part of the function* of PCI control signals, *such as* FRAME#, IRDY#, and TRDY#," (*id.* at 21:55-58 (emphasis added)). By referring to "part of the function of PCI control signals" instead

of simply referring to "PCI control signals," the specification indicates that the invention does not require the PCI control signals themselves. Ex. 16, Levitt Decl. ¶¶ 32, 91. Instead, the invention replaces PCI control signals with different information that may perform a similar function, *e.g.*, to allow backward compatibility.[8] *Id.* The specification's description of information conveyed over the XPBus does not include any of the other parallel PCI bus signals listed in Figure 16, such as PAR (parity), at all. Ex. 1, '768 patent at 21:37-22:42. As recognized by Judge Davis:

> [O]ne of skill in the art would conclude that the term PCI bus in the patent is not specific to a PCI Local Bus Standard form of architecture and that a 'PCI bus transaction' is used to merely designate[] an ability to communication with a legacy device (i.e., an interconnected peripheral that is designed to operate over a conventional PCI Local bus) so that backward compatibility with an installed base of peripherals is assured.

Appro, 2011 U.S. Dist. LEXIS 10515, at *25.

2. ACQIS's proposed construction of "PCI bus transaction" aligns with the way the PCI industry specifications describe a "transaction."

While Defendants argue that ACQIS's proposed construction of the claim language departs from the plain and ordinary meaning of "transaction" (Dkt. 77 at 10), the PCI Specification supports ACQIS's construction. It uses the term "transaction" to describe address, data, command, and byte enable information, consistently with its usage in the ACQIS patents. Ex. 16, Levitt Decl. ¶¶ 33-36, 75. The PCI Specification glossary defines a "transaction" as "an address phase plus one or more data phases." Ex. 18, PCI 2.1 at 272; Ex. 19, PCI 2.2 at 301; Ex. 16, Levitt Decl. ¶ 76. It defines a "phase" as "[o]ne or more clocks in which a single unit of *information* is transferred." Ex. 18, PCI 2.1 at 271 (emphasis added); Ex. 19, PCI 2.2 at 300; Ex. 16, Levitt Decl. ¶ 77.

[8] The claims at issue do not recite the XPBus control information described in this embodiment.

The PCI Specification also describes command and byte enable information transferred during the address and data phases of a "transaction": "During the address phase of a transaction, C/BE[3::0]# define the bus command . . . . During the data phase, C/BE[3::0]# are used as Byte Enables." Ex. 18, PCI 2.1 at 9, 21; Ex. 19, PCI 2.2 at 9-10, 21; Ex. 16, Levitt Decl. ¶ 76.

A POSITA reading a patent about a new physical interface invention and referencing the PCI Specification would understand from these definitions and descriptions that a PCI "transaction" (when not further limited) refers to the information communicated in the address phase and data phase (Ex. 16, Levitt Decl. ¶¶ 77-78)—in other words, the address bits plus command bits and the data bits plus byte enable bits–the actual activity of the communication interchange. There would be no need for the control signals used to communicate that information over a specific parallel PCI bus or other information communicated outside the address and data phases. *Id.* ¶¶ 79, 85-90, 93-94. The PCI Specification describes control signals as separate from a "transaction." Ex. 18, PCI 2.1 at 269; Ex. 19, PCI 2.2 at 297; Ex. 16, Levitt Decl. ¶¶ 86-87. It also describes other information, like a "parity" bit (sent *after* the "transaction" to confirm that the "transaction" occurred properly), as distinct from the "transaction" itself. Ex. 18, PCI 2.1 at 95-96, 250; Ex. 19, PCI 2.2 at 93-95, 255; Ex. 17, Levitt Rebuttal Decl. ¶¶ 5-9.

3. Defendants' proposed construction lacks sufficient detail to resolve any dispute and conflicts with the intrinsic record and extrinsic evidence.

Defendants' proposed construction for "PCI bus transaction"—"a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"—either says far too little to resolve any dispute or narrows the claims far too much—so much that it undermines the whole point of the invention. Defendants urge the Court to follow the *EMC* construction since the parties in *EMC* agreed to this construction. However, as discussed in detail in Section III.A.6, that court's application of

the construction at summary judgment altered it beyond the parties' agreement, which shows that the construction itself does not provide enough clarity to resolve potential disputes, and, in any event, is not binding on this Court or on ACQIS.

If Defendants' construction limits the term "PCI bus transaction" to the "entirety" of the PCI Specification, as the *EMC* court ultimately found, then it plainly conflicts with the express claim language of the patents-in-suit and the embodiments in the intrinsic record demonstrating that many embodiments of the claimed inventions do not require the presence of a parallel PCI bus or its corresponding control signals. *See* Section III.A.1-2, 5; *see also Phillips*, 415 F.3d at 1314 (requiring construction consistent with context of claim language itself); *Eko Brands, LLC v. Adrian Rivera Maynez Enterprises, Inc.*, 946 F.3d 1367, 1373 (Fed. Cir. 2020) (finding error in a proposed construction that would exclude "embodiments in the specification"). Judge Davis's 2011 *Markman* Order confirms that a "PCI bus transaction" does ***not*** require every aspect of a parallel PCI bus because the invention replaces that interface: "Therefore, consistent with Acqis's arguments, the 'PCI bus transaction' allows compatibility with PCI legacy devices when replacing the conventional parallel PCI bus with a serial architecture." *Appro*, 2011 U.S. Dist. LEXIS 10515, at *24.

In addition, construing "PCI bus transaction" to require the entirety of the PCI Specification would be overly broad and nonsensical, since that specification relates to many things other than just "transactions." For example, it also relates to electrical requirements such as "Maximum AC Ratings and Device Protection" (Ex. 19, PCI 2.2 at 120), pin capacitance and voltage (*id.* at 122); power requirements, such as the number of power rails for each connector and current requirements (*id.* at 137); physical requirements such as "Routing and Layout Recommendations for Four-Layer Boards," "Planar Impedance," and "Connector Pin

Assignments" (*id.* at 236); and many other requirements. Construing "PCI bus transaction" to require implementation of the entirety of the PCI Specification would have the absurd result of including each of these requirements and all other requirements detailed in the approximately 300 pages of the specification.

If, instead, Defendants' intend their construction to require less than the "entirety" of the PCI Specification, then it provides no clarity on what a "PCI bus transaction" does or does not require. In the *Samsung* litigation, ACQIS discussed statements by Samsung's expert, Dr. Colwell, to provide an example of the confusion resulting from a construction requiring only unspecified aspects of the PCI Specification. Ex. 29, *Samsung*, No. 2:20-cv-00295-JRG, Dkt. 65 at 12-13 (E.D. Tex. Aug. 23, 2021). Dr. Colwell contended that a POSITA would look at "all relevant aspects" of the PCI Specification to understand (1) what "transaction" means in the context of the PCI Specification and (2) what is required to practice the claims. Ex. 24, Colwell Decl. ¶ 58; Ex. 25, Colwell Rebuttal Decl. ¶ 9. "All *relevant* aspects" are less than all aspects of the PCI Specification in its entirety, but without more detail, that phrase would not tell a POSITA anything about which aspects are "relevant."

4. The intrinsic record and extrinsic evidence show that a "PCI bus transaction" does not require "parity," "control signals," or "address and data phases."

Defendants agree that a "PCI bus transaction" includes at least the information in ACQIS's construction. *See, e.g.*, Dkt. 77 at 18. However, Defendants identify three other things that a "transaction" purportedly requires: "control signals," "parity," and "address and data phases." *Id.* at 12-15. Defendants argue that the "transaction requires more" but fail to include any of these items in their proposed construction and ignore that ACQIS's construction, rather than being limiting, requires "at least" PCI address data, byte enable, and command type information. *Id.* at 13.

Defendants do not—and cannot—dispute that, while the claims reference the information in ACQIS's proposed construction (i.e., address, data, and byte enable information), they do not recite "address and data phases," "control signals," or "parity." Defendants also do not dispute that Figure 13 of the '768 patent illustrates a "PCI bus transaction" using the invention's XPBus and expressly includes the four types of PCI information in ACQIS's proposed construction. Defendants do not dispute that Figure 13 does not expressly illustrate any PCI "control signals" or "parity," such as the signals in Figure 16 describing the prior parallel PCI bus, nor do they contrast Figures 13 and 16. In fact, Defendants never substantively discuss Figure 13 at all. Rather, Defendants rely on Figure 16 to argue that the specifications do not limit a "PCI bus transaction" to the types of information identified by ACQIS, disregarding that Figure 16 represents the prior parallel PCI bus and not the invention. Dkt. 77 at 16. In other words, Defendants' reliance on Figure 16 undermines their position.

The '768 patent's specification also contradicts Defendants' position by illustrating a "PCI bus transaction" without requiring any parallel PCI control signals. The specification states that "BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus," and they indicate XPBus functions like "idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles." Ex. 1, '768 patent at 21:40-47, 21:59-63. These bits represent new status information for the invention's new interface channel, not implicit PCI signals.

The specification further states that in "one embodiment," BS0-BS3 represent "*part* of the *function* of PCI control signals, *such as* FRAME#, IRDY#, and TRDY#." Ex. 1, '768 at 21:37-58 (emphasis added). That is, BS0-BS3 do not represent *all* PCI control signals and are not *themselves* PCI control signals. They may or may *not* represent FRAME#, IRDY#, and

TRDY#, as indicated by the permissive exemplary language "such as." If BS0-BS3 represent a PCI signal at all, they clearly need not represent *all* the functionality of any signal.

Finally, in "one embodiment," "BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively." *Id.* at 22:31-32. That is, BS0-BS3 may, but not *must*, represent PCI control signals. This embodiment omits TRDY#, which Defendants incorrectly assert is necessarily present in BS0-BS3, demonstrating that Defendants' inference is wrong. Defendants fail to address any of these embodiments.

As to "parity," Defendants do not identify anything from the intrinsic record suggesting that a "PCI bus transaction" requires "parity," even by inference. Defendants also do not address that the "PCI bus transaction" described in Figure 13 does not reference "parity" at all. Defendants have no intrinsic support for requiring "parity" in claim language lacking that term. Dkt. 77 at 15-17.

The extrinsic evidence also contradicts Defendants' position. The PCI Specification explains that "parity is calculated . . . *on* all PCI transactions," not that it is *part of* the transaction. Ex. 19, PCI 2.2 at 94 (emphasis added), 255; Ex. 17, Levitt Rebuttal Decl. ¶¶ 6-9. The statement Defendants' quote for their position—"[d]uring address and data phases, parity covers AD[31::00] and C/BE[3::0]# lines"—does not say that parity is part of a "transaction"—it does not even use the term "transaction." Dkt. 77 at 16. That parity is *calculated on* a "transaction" during a "transaction" instead shows that it is separate and different from the transaction itself, even if it occurs at the same time.

Defendants try to introduce "address and data phases" as implied parts of the construction, but fail to provide any intrinsic evidence that "address and data phases" are themselves included in a "PCI bus transaction" rather than simply phases during which the

information of the "transaction" is transferred. The PCI Specification describes how command type and byte enables are part of a transaction *during* the address and data phases. "During the address phase of a transaction, C/BE[3::0]# define the bus command:. . . . During the data phase, C/BE[3::0]# are used as Byte Enables." Ex. 18, PCI 2.1 at 9; *see also id.* at 21; *see also* Ex. 19, PCI 2.2 at 9-10, 21; *see also* Ex. 16, Levitt Decl. ¶ 76. A phase is one or more clock cycles in which information is transferred. Ex. 18, PCI 2.1 at 271; *see also* Ex. 19, PCI 2.2 at 300; *see also* Ex. 16, Levitt Decl. ¶ 77. Accordingly, a POSITA would understand that a "transaction" according to the PCI Local Bus Specification (when considering an invention that is designed to replace the old physical structure) is the *information* communicated in the address phase and data phases, which aligns with how that term should be construed in the context of the patents-in-suit. Ex. 18, PCI 2.1 at 9, 271-272; *see also* Ex. 19, PCI 2.2 at 9-10, 300-301 *see also* Ex. 16, Levitt Decl. ¶ 78.

5. ACQIS's construction is consistent with its positions at the PTAB.

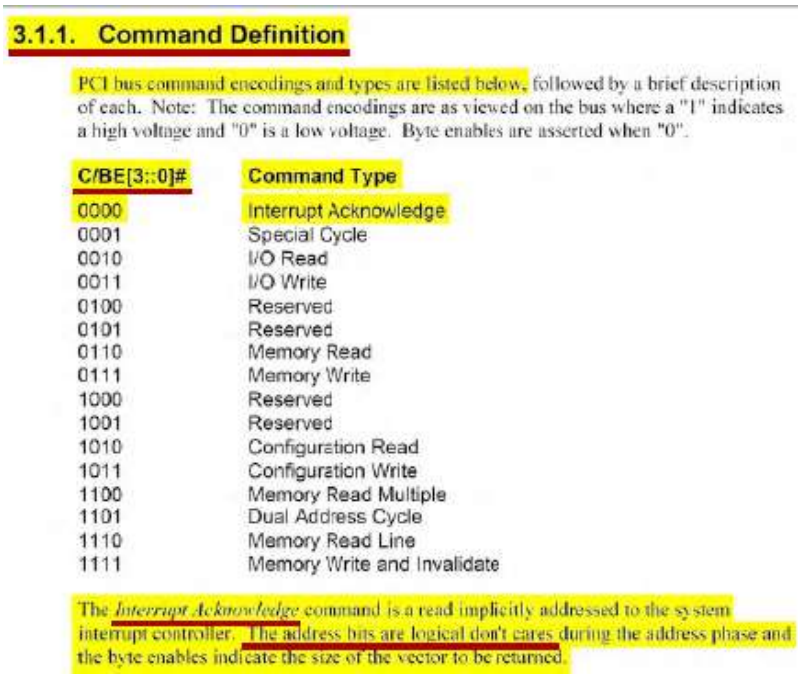
Before the PTAB, as here, ACQIS contended that a "PCI bus transaction" should be construed in accordance with the information required by the PCI Specification. ACQIS's construction specifies what information is required to resolve the parties' dispute.

Defendants are wrong that ACQIS's current construction excludes "control bits" discussed in the PTAB. During IPR oral argument, ACQIS's counsel used the term "control bits" to refer to the command information ACQIS has proposed here, explaining:

> The piece we are looking at is Section 3.1.1., Command Definition…So keep in mind the PCI standard has two timing requirements and they have what they call a data phase which the data is transmitted, so it's a time, and then the address phase. And **in the address phase they send the address and the control bits**. So during that phase the control bit, if it's an **interrupt acknowledge**, you can see that the address bits are don't cares.

Ex. 26, *EMC Corp. v. ACQIS LLC*, IPR2014-01469, Paper No. 55 at 37:15-38:2 (PTAB Jan. 5,

2016) ("IPR2014-01469") (emphasis added). The reference to the "Command Definition" of the PCI Specification makes this clear because that section refers to command type information, not "control signals" like FRAME#, IRDY#, or TRDY#:



3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

The *Interrupt Acknowledge* command is a read implicitly addressed to the system interrupt controller. The address bits are logical don't cares during the address phase and the byte enables indicate the size of the vector to be returned.

Ex. 19, PCI 2.2 at 21 (highlighting and underlining added). Moreover, ACQIS's IPR counsel's statement aligns with the PCI Specification's explanation that "[d]uring the address phase of a transaction, C/BE[3::0]# define the bus *command*." Ex. 19, PCI 2.2 at 9-10 (emphasis added). It further explains that "Interrupt Acknowledge" is a "Command Type" defined by the value "0000" for the bits C/BE[3::0]#. *Id.* at 21. ACQIS's counsel therefore described the invention consistent with ACQIS's proposed construction here, which includes "command type information."

In addition, when read as a whole (rather than the selective cherry picking done by Defendants), the testimony of ACQIS's IPR expert, Dr. Lindenstruth (Dkt. 77 at 17) is consistent with a "transaction" not including the control signals themselves. In a later part of his deposition not quoted by Defendants, Dr. Lindenstruth confirmed that the PCI Specification supported his

construction of "PCI bus transaction" as set out in his declaration from the IPR of the '873 patent. Ex. 27, IPR2014-01469, Dep. Trans. of V. Lindenstruth at 350:25-351:10. There, he explained, "the claims do not require that the PCI bus transaction occur on a PCI bus; they require the address and data phases of a PCI bus transaction, which include the PCI *address and bus command information* during the address phase, and the PCI *data and byte enables* during the data phases." Ex. 28, IPR 2014-0162, Declaration of V. Lindenstruth ¶ 114 (emphasis added). It is well settled that a statement that is ambiguous or subject to more than one reasonable interpretation does not constitute clear and unmistakable disclaimer. *Sandisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1287 (Fed. Cir. 2005) (holding that district court erred in claim construction finding of disclaimer; vacated and remanded). These statements, which are consistent with ACQIS's proposed construction of "PCI bus transaction" that does not require control bits themselves, cannot constitute unequivocal disavowal of claim scope.

6. The district court's construction in *EMC* does not compel the same construction here.

Defendants argue that the *EMC* court has already rejected ACQIS's proposed construction of "PCI bus transaction," and ACQIS is estopped from even raising this issue in these proceedings. However, the *EMC* court's construction of "PCI bus transaction" does not require the same construction here. The *EMC* court did not address the same issue as here: the proper construction, under *Phillips*, of "Peripheral Component Interconnect (PCI) bus transaction" based on the intrinsic record of the different claims asserted in this case and relevant extrinsic evidence. Moreover, the construction was for a term that is different from the claim term at issue here. In this litigation, the parties have asked the Court to construe "PCI bus transaction," but, as the EMC court acknowledged, ACQIS and EMC agreed to construe "transaction" and "Communicating…PCI bus transaction." *EMC I*, 2017 U.S. Dist. LEXIS

202160 at *9, *26.

In *EMC* the court adopted language stipulated to by the parties: "a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component." *EMC I*, 2017 U.S. Dist. LEXIS 202160, at *9 (discussing language agreed to by the parties), *14-15 (adopting language). The court thus did not need to evaluate the intrinsic record to determine which aspects of the PCI Specification the claims required. *Id.* at *9-10. Based on the issues presented, the court analyzed the intrinsic record only to address additional language proposed by EMC that would require the presence of a parallel PCI bus, and the court concluded the construction should not require a PCI bus. *Id.*

At summary judgment, however, EMC argued that the stipulated construction required compliance with the PCI Specification "in its entirety," and the court, applying the construction, found for the *first time* that the claims required "every element" of the PCI Specification—"the claims are limited by the Specification in its entirety." *EMC II*, 2021 U.S. Dist. LEXIS 55945 at *11-19. The court did not analyze the intrinsic or extrinsic evidence in reaching this new claim construction conclusion, and instead found that ACQIS's arguments about the intrinsic record were an "attempt[] to reopen claim construction" and "untimely." *Id.* at *14. The *EMC* court thus appeared to base its conclusions on a finding that ACQIS forfeited its arguments by not presenting them in a timely fashion, not on an interpretation of the claims under the *Phillips* standard.[9] *See In re Google Tech. Holdings LLC*, 980 F.3d 858, 862 (Fed. Cir. 2020) (explaining "forfeiture is the failure to make the timely assertion of a right").

The *EMC* court's construction, as interpreted in the summary judgment order, does not mandate the same construction here. *See, e.g.*, *State Farm Mut. Auto. Ins. Co. v. LogistiCare*

[9] ACQIS has appealed the *EMC* matter to the Federal Circuit and has filed its opening brief.

Solutions, LLC, 751 F.3d 684, 689 (5th Cir. 2014) (explaining that issue preclusion requires actual litigation of identical issues). First, a claim construction adopted by stipulation in one case does not have preclusive effect in a later case, so there can be no collateral estoppel. *See Pfizer, Inc. v. Teva Pharms., USA, Inc.*, 429 F.3d 1364, 1375-76 (Fed. Cir. 2005) (refusing to apply stipulated construction, from prior case, to the same patent claims in later case); *Allergan Sales, LLC v. Sandoz Inc.*, No. 2:12-cv-207-JRG, 2016 U.S. Dist. LEXIS 41013, at *21 (E.D. Tex. Mar. 29, 2016) (finding that issue preclusion did not arise from stipulated construction). The *EMC* court's application of the stipulated construction, without consideration of the intrinsic record, therefore also cannot have preclusive effect here.

Second, there is no collateral estoppel from the *EMC* case because the Federal Circuit has not affirmed the district court's constructions. Defendants quote *Phil-Insul Corp. v. Airlite Plastics Co.*, 854 F.3d 1344 (Fed. Cir. 2017) to show the requirements of collateral estoppel, but they use an ellipse to disingenuously gloss over one unsatisfied, but essential, factor: finality. *Id.* at 1357-58 ("the claim construction became final when we [Federal Circuit] affirmed them on appeal."). Defendants cannot dispute that the appeal of the *EMC* claim constructions is still pending, and they have not been affirmed. Since the *EMC* constructions are not final, they cannot constitute collateral estoppel.

Third, although ACQIS agreed to the *language* of the *EMC* court's construction, it did not agree to the court's further *interpretation* of that language requiring the PCI Specification "in its entirety." The *EMC* summary judgment order makes that clear, describing ACQIS's arguments in opposition and dismissing them as "untimely." *EMC II*, 2021 U.S. Dist. LEXIS 55945, at *14. The *EMC* court thus did not address the merits of ACQIS's arguments regarding the proper scope of the parties' stipulated construction, and thus the issue was not actually

litigated for collateral estoppel purposes.

Fourth, the *EMC* court's analysis does not inform, even as persuasive authority, the proper construction of "PCI bus transaction" based on the claim language and disclosures of the different patents and claims asserted in this case. For example, the *EMC* court did not address the phrases at issue here reciting only certain bits of a "PCI bus transaction," including "address and data bits of a Peripheral Component Interconnect (PCI) bus transaction" or "address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction." *See, e.g.*, Ex. 2, '750 patent at 40:39-43 (claim 1), 41:3-7 (claim 5). The *EMC* court also did not address the teachings of Figure 8B, which illustrates the invention's interface channel connected directly to a chip without a parallel PCI bus. Ex. 1, '768 patent at Fig. 8B. That embodiment would be improperly excluded if the *EMC* claim construction were adopted and applied. *Eko Brands*, 946 F.3d at 1373 (refusing to adopt proposed construction that would exclude embodiments).

Neither the *EMC* claim construction order nor its interpretation of "PCI bus transaction" at summary judgment addressed the claim language or intrinsic record for the ACQIS claims asserted here. Since the parties in the *EMC* litigation did not actually litigate the claim term at issue in this litigation in the context of the claims at issue here, the *EMC* court's claim interpretations cannot constitute collateral estoppel. Once the Court performs its own analysis based on the intrinsic record, it will find that it should adopt ACQIS's proposed construction of "PCI bus transaction."

B. Terms reciting "address and data bits" or "address bits, data bits, and byte enable information bits" of a PCI bus transaction

ACQIS's Construction	Defendants' Construction
No construction needed.	A PCI bus transaction, including all address,

These phrases recite the bits of a PCI bus transaction that are conveyed / transmitted / communicated, *i.e.*, "address bits," "data bits," and "byte enable information bits," as applicable. Claims that recite these bits do not require that other, non-recited bits be conveyed / transmitted / communicated. The claims, as written, are clear, and this language of the claims does not require construction.	data, and control bits.

As discussed above, a PCI bus transaction (when not further limited by the claim language) includes at least PCI address bits, data bits, byte enable information bits, and command bits. Some claims recite specific bits in each individual claim: "address bits," "data bits," and/or "byte enable information bits," depending on the claim. These terms need no further construction and certainly do not need to add "control bits."

To Defendants, this express claim language should be ignored. Defendants propose to construe the claims, no matter which bits they recite, as requiring "a PCI bus transaction, including all address, data, and control bits." Defendants' proposed construction plainly conflicts with the express claim language and improperly renders it superfluous. *See Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.") It also conflicts with the specifications' disclosures to the extent the construction requires all control signals used for a prior art parallel PCI bus, because it would exclude the embodiments that do not require those signals. *See* Sections III.A.3, 6; *Eko Brands*, 946 F.3d at 1373 (refusing to adopt proposed construction that would exclude embodiments). And it violates the presumption of claim differentiation. *See Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008) (declining to construe different claims terms as having the same meaning where Federal Circuit "precedent instructs that different claim terms are ***presumed*** to have different

meanings") (emphasis added).

Again, the *EMC* case does not justify Defendants' construction. Defendants' proposed construction tracks the language the parties in *EMC* agreed upon for the phrase "[c]ommunicating . . . PCI bus transaction." *EMC I*, 2017 U.S. Dist. LEXIS 202160, at *5, *25-26. The *EMC* court did not address the claim language or intrinsic record relating to this term, either in its claim construction order or at summary judgment. *Id.*; *see also EMC II*, 2021 U.S. Dist. LEXIS 55945, at *14-15. For the reasons discussed above with respect to "PCI bus transactions," the agreed-upon construction in *EMC* does not determine the correct construction here, particularly in view of the significant conflicts between the *EMC* construction, the claim language, and the intrinsic record for the claims at issue here.[10] ACQIS's agreement to a construction including "control bits" in *EMC* for different phrases does not show that ACQIS conceded to Defendants' contention "that control signals such as FRAME# form a necessary part of the claimed PCI bus transaction." DKT 77 at 15 (emphasis added). Defendants do not dispute the fact that the parties agreed to a construction that has no preclusive effect.

Defendants never address the difference in scope between claims that recite specific bits of a "PCI bus transaction" and claims that do not. Instead, Defendants lump these differently drafted claims together and argue that ACQIS disclaimed any difference in scope during IPR. However, as explained in Section III.A.5, none of these statements amount to unambiguous and unmistakable disclaimer when considered in context.

C. "encoded" / "serial"

ACQIS's Construction	Defendants' Construction

[10] In addition, the *EMC* record indicates that the parties disagreed about the meaning of "control" bits: ACQIS understood that term to mean PCI command bits, while EMC interpreted it to mean PCI bus control signals. ACQIS's constructions here avoid introducing such ambiguity.

"encoded": Code representing a PCI bus transaction. Claims reciting an "encoded" PCI bus transaction or PCI bus transaction in "serial stream" or "serial form": PCI bus transaction in serial form.	A PCI bus transaction that has been serialized from a parallel form.

For phrases including the terms "encoded" and "serial," the parties dispute whether those phrases recite commonly understood terms in the field of computer science (ACQIS's position) or whether they instead require performing parallel-to-serial conversion on a PCI bus transaction originating from a parallel PCI bus (Defendants' position). Once again, Defendants' construction would introduce a parallel PCI bus into all claims that mention "PCI."

1. The term "encoded" does not require parallel-to-serial conversion of a parallel PCI bus transaction.

"Encoded" bits simply refers to a coded representation of bits, as ACQIS has proposed. "Encode" has an ordinary meaning in computing: "[t]o express a single character or message in terms of a code." Ex. 20, IEEE Dictionary, 6th ed., at 355. For serial data transmission specifically, "encoding" means "[t]he representation of data bits and nondata information for the purpose of signal transmission across a serial communications medium." *Id.* ACQIS has done nothing to alter this ordinary meaning.

The claims at issue recite specific bits in "encoded" form. For example, claim 4 of the '768 patent recites "encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction." Ex. 1, '768 patent at 41:1-7. These limitations, applying the ordinary meaning of "encoded," refer to a coded representation of certain information (address and data bits, in claim 4 of the '768 patent) of a PCI bus transaction. Ex. 16, Levitt Decl. ¶ 36.

ACQIS's proposed construction accords with these well-recognized meanings and Judge Davis's prior construction of "encoded PCI bus transaction": "code representing a PCI bus

transaction." *Alcatel-Lucent*, 2015 U.S. Dist. LEXIS 48339, at *17. Judge Davis found that "an encoded PCI bus transaction does not require any parallel-to-serial conversion at all." *Id.* at *16. The Court noted that the claim language at issue—reciting "a central processing unit directly connected to a first [LVDS] channel to convey a first encoded serial bit stream of address and data bits of a [PCI] bus transaction"—"suggests that an encoded PCI bus transaction does not require any parallel-to-serial conversion at all." *Id.* Judge Davis also concluded that the specification "discloses 'encoding' in a context that is not tethered to parallel-to-serial conversion." *Id.* (citing Ex. 5, '873 patent at 5:34-48). Judge Davis's construction should be given greater weight than the *EMC* construction for the reasons discussed below, but also because that construction was legally determined by the court rather than stipulated to by the parties, was used in a jury trial, and was not disturbed on appeal.

The claims at issue here likewise recite a chip (either a "central processing unit" or a "peripheral bridge") "directly connected to" a channel (or a channel "directly extending from" a chip) to convey "encoded" bits. *See, e.g.*, Ex. 2, '750 patent at 40:36-49 (claim 1), 41:1-15 (claim 5). The claims do not recite parallel-to-serial conversion. By reciting bits conveyed "directly" from a chip, they indicate that the bits never had to exist as part of a PCI bus transaction in parallel form requiring conversion. Ex. 16, Levitt Decl. ¶¶ 113-115.

The specifications at issue here contain the same disclosure that Judge Davis cited in refusing to read parallel-to-serial conversion into "encoded." *Compare* Ex. 5, '873 patent at 5:34-48 *with* Ex. 1, '768 patent at 5:50-65 (reciting identical disclosures). The specifications here also include embodiments, such as Figures 8A and 8B, illustrating the invention's LVDS channel "directly connected" to a chip with no parallel-to-serial conversion or any parallel interface such as a PCI bus. Ex. 1, '768 patent at Fig. 8A, Fig. 8B, 15:57-16:36; Ex. 6, Levitt Decl. ¶¶ 112-117.

Further, in embodiments that also provide parallel-to-serial conversion, the ACQIS patents, including the '873 patent, describe "encod[ing]" as a separate and different process. Ex. 16, Levitt Decl. ¶ 119. Figure 10 of the '768 patent, for example, illustrates an embodiment that includes a parallel "host PCI bus." Ex. 1, '768 patent at Fig. 10, 17:44-46; Ex. 16, Levitt Decl. ¶110.

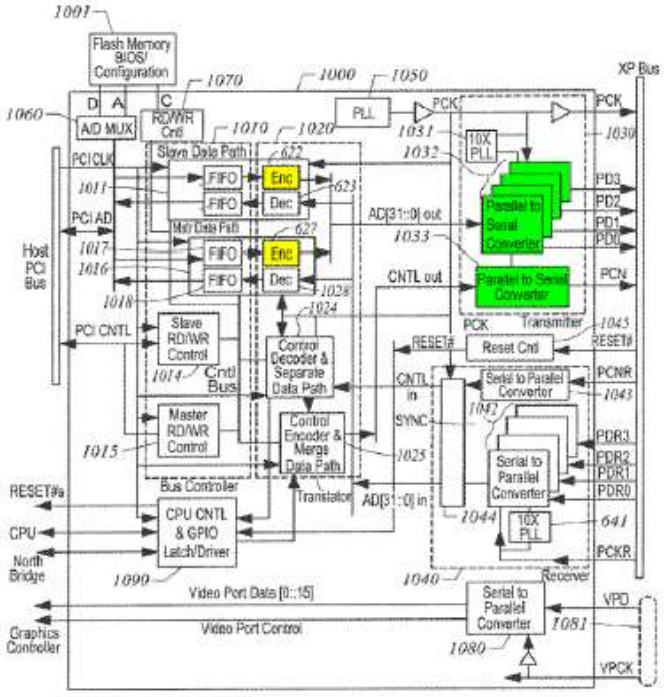


FIGURE 10

This embodiment illustrates and describes "encoders" that are entirely separate and distinct from "parallel-to-serial converters." Ex. 1, '768 patent at Fig. 10, 17:56-64 (describing "encoders"), 18:63-19:17; Ex. 16, Levitt Decl. ¶ 119. In this embodiment, the "encoders" "format the PCI address/data bits to a form more suitable for parallel to serial conversion." Ex. 1, '768 patent at 17:59-64. They do not *themselves* perform parallel-to-serial conversion. They instead prepare a coded representation of address and data bits, consistent with ACQIS's construction and with Judge Davis's construction. The parallel-to-serial converters perform the conversion operation, demonstrating that the term "encoded" does not require this process. *Id.* at 18:63-19:2.

Defendants briefly refer to the embodiment shown in Figure 10 but fail to recognize that the encoders and serial converters are separate processes. Dkt. 77 at 30-31.

"Encoded" thus has an ordinary meaning, and the claims and specification use "encoded" consistent with that meaning. To adopt Defendants' narrow construction—"a PCI bus transaction that has been serialized from a parallel form"—would require a clear intent on the part of the patentee to define "encoded" with a special meaning or to disclaim scope otherwise covered by the ordinary meaning. *Phillips*, 415 F.3d at 1316. Neither limiting principle applies here.

Further, the EMC court's construction of phrases including the word "encoded" does not compel a narrower construction here. There, the district court construed "[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms." *EMC I*, 2017 U.S. Dist. LEXIS 202160, at *25. The *EMC* court's rationale depended on finding prosecution disclaimer arising from IPR proceedings addressing the '873 and '814 patents, one of which—the '814 patent—is not at issue in this case. *Id.* at *2 (listing patents), *22-25 (analyzing disclaimer).

Defendants argue that ACQIS disavowed claim scope during IPR when it made statements about embodiments in which bits in parallel form are converted to serial form and then back to parallel form (*e.g.*, "one key to the invention was to serialize the otherwise parallel PCI bus transactions" and referring to the serialization of the parallel bits being like an "hourglass"). Dkt. 77 at 27-28. Serialization can refer to complete serialization of the prior parallel standard with no remaining parallel bus. While some embodiments have parallel-serial-parallel conversion, ACQIS also has claims that do not include that requirement. ACQIS could have limited its specification and claims to embodiments that require parallel-serial-parallel conversion, but it did not do so. *See, e.g.*, Ex. 1, '768 patent, Fig. 10 (showing embodiment with

separate encoders, parallel to serial converters, and serial to parallel converters).

The prosecution disclaimer found in *EMC* for the '873 and '814 patents does not apply to the different patents asserted here, which include different claim language and disclosures. *See Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1323 (Fed. Cir. 2013) (finding that prosecution disclaimer did not attach to patent family member based on the family member's intrinsic record).[11] For example, the '873 and '814 patents for which the *EMC* court found disclaimer do not include Figures 8A and 8B, a key embodiment corresponding to the great majority claims here, that illustrate a serial LVDS channel direct from a chip with no parallel interface. Ex. 5 ('873 patent); Ex. 23 ('814 patent). Those disclosures "directly contradict" the *EMC* prosecution disclaimer finding, and therefore that finding does not attach to the patents-in-suit disclosing that embodiment. *Trading Techs.*, 728 F.3d at 1323.

Regardless of its applicability, the *EMC* court's finding of prosecution disclaimer was wrong. The '873 patent contains Figure 10, which discloses an embodiment of the invention clearly showing that encoding and parallel-to-serial conversion are separate functions. The '814 patent discloses a similar embodiment in Figure 12a, which also clearly shows encoding and parallel-to-serial conversion as separate functions. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (finding that a construction that excludes an embodiment is "rarely, if ever, correct"). In addition, the specification states: "Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus." Ex. 5, '873 patent at 16:55-58. Defendants quote this sentence but it

[11] In addition, the '984, '602, '468, '654, '739, '140, and '947 patents asserted here do not claim priority to either the '873 or '814 patents, so the *EMC* prosecution disclaimer finding cannot attach. *Trading Techs.*, 728 F.3d at 1323 ("Prosecution history estoppel can extend from a parent application to subsequent patents in the same lineage, . . . as can prosecution disclaimer . . . .") (citations omitted).

does not actually support their position since it references formatting of the bits and serial conversion as two separate things. Dkt. 77 at 31. The Court should therefore construe "encode" as its own term without conflating it with parallel-to-serial conversion.

2. The term "serial" does not require parallel-to-serial conversion of a parallel PCI bus transaction.

The term "serial" in the claims also does not require parallel-to-serial conversion for similar reasons. The claims do not recite a set of bits in parallel form that would require conversion. They also do not recite a parallel bus that would require conversion to transmit corresponding bits over a serial channel. Instead, the claims recite "serial" terms to describe *how* the recited bits (such as address and data) are conveyed or transmitted. For example, claim 1 of the '768 patent recites "a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller *to convey* address and data bits of a Peripheral Component Interconnect (PCI) bus transaction *in a serial form*." Ex. 1, '768 patent at 40:41-49 (claim 1) (emphasis added). This claim language would apply regardless of whether there was a prior conversion from a parallel format or if the information was natively serial.

The specifications describe parallel-to-serial conversion only in the context of embodiments that include a parallel PCI bus. *Id.* at 17:29-46, 18:63-19:2, Fig. 10 (describing parallel-to-serial conversion in "one embodiment" that includes a "host PCI bus"). They do not define "serial" as always requiring parallel-to-serial conversion. "Serial" has an ordinary meaning in the field of data transmission: "one bit at a time on a single path." Ex. 20, IEEE Dictionary, 6th ed., at 971 (defining "serial transmission" as "the conveying of a character of information one bit at a time on a single path"); *see also, e.g.*, *id.* at 970-71 (defining "serial" as "[o]ne bit following another over a single pathway"; defining "serial interface" as "[a]n interface that transmits data bit by bit rather than in whole bytes"). The intrinsic record for the patents-in-

suit is consistent with and does not include any unambiguous deviation from this plain and ordinary meaning of "serial." ACQIS's proposed construction is also consistent with Judge Davis's previous construction of the term "[in a] serial bit stream": "a flow of information in which units of information are transferred serially from one component to another." *Alcatel-Lucent*, 2015 U.S. Dist. LEXIS 48339, at *9.

Defendants' construction of the disputed phrases including "encoded" and "serial" terms—which Defendants contend should apply whether "encoded" appears in a claim or not—would improperly limit the claims to embodiments in which a PCI bus transaction originates from a parallel PCI bus. *See C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 865 (Fed. Cir. 2004) (refusing to limit claims to specific embodiments). The construction would improperly narrow the ordinary scope of "encoded" and "serial" without support from any unambiguous definition or disavowal of claim scope in the intrinsic record. *See Phillips*, 415 F.3d at 1316 (describing requirements of "special definition" or "intentional disclaimer" to limit ordinary meaning). Again, this position contradicts one of the fundamental reasons for the invention to obviate the need for a parallel bus. Absent clear statements in the specification or prosecution history that an invention is limited in a particular way, it is improper to import particular embodiments into the claims. *Hill-Rom Servs. v. Stryker Corp.,* 755 F.3d 1367, 1372-73 (Fed. Cir. 2014) (holding that district court erred by importing limitation from specification into claims). None of the statements from the intrinsic record quoted by Defendants come close to showing a clear intent to narrow claim scope. None of them define encoding or serializing in terms of each other, and most do not even refer to both processes in the same sentence. Those that do indicate that encoding and serializing are separate processes. Dkt. 77 at 31-32, citing Ex. 5, '873 patent at 17:8-13.

Finally, Defendants' proposed construction would improperly exclude the embodiments in Figures 8A and 8B of the '768 patent that do not include a PCI bus or any other parallel interface prior to serial transmission across the interface channel. *See Vitronics Corp.*, 90 F.3d at 1583. Defendants likely realize that their proposed construction would improperly exclude the embodiments of Figures 8A and B because those embodiments are the main targets of three IPR petitions filed by Intel in which Lenovo is the real party of interest. *See Intel Corp. v. ACQIS, LLC*, IPR2021-01107, IPR2021-01108, and IPR2021-01109 (PTAB Jun. 14, 2021).[12] Samsung made substantially the same arguments in earlier filed IPR petitions filed against the '768 and '750 patents, but the PTAB rejected those arguments and denied institution with respect to both patents. *See Samsung Elec. Co., Ltd. v. ACQIS LLC*, IPR2021-00604, Paper No. 7 (PTAB Aug. 9, 2021); *Samsung Elec. Co., Ltd. v. ACQIS LLC*, IPR2021-00605, Paper No. 7 (PTAB Aug. 23, 2021).

D. Terms reciting "Universal Serial Bus (USB) protocol"

ACQIS's Construction	Defendants' Construction
"Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol data": USB data payload. "Universal Serial Bus (USB) protocol information": Information described in the USB specification.	[Data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification.

Several ACQIS claims recite using the invention's new LVDS interface channel to convey "Universal Serial Bus (USB)" protocol data or information. The specifications contemplate that the invention's serial LVDS channels can improve existing buses other than PCI, such as USB. *See, e.g.*, Ex. 1, '768 patent at 25:8-12 (explaining that the invention can

[12] ACQIS filed responses to these petitions on September 17, 2021.

"support non-PCI bus transactions, e.g., USB transactions"), 5:47-49 (describing invention for "PCI-like buses"), 6:1-3 (same), 18:59-62 (same). The Court should adopt ACQIS's proposed constructions because they accord with both the intrinsic and extrinsic evidence.

By contrast, Defendant's proposed construction is an attempt to improperly narrow the scope of the USB terms, as they did with regard to the PCI terms, to require conveying full USB transactions, regardless of the specific language of each claim. Defendants' proposed construction improperly limits the claims and renders certain expressly recited terms superfluous. It should be rejected on at least those bases.

1. ACQIS's proposed constructions of the "USB" claim terms is consistent with the intrinsic and extrinsic evidence.

"Universal Serial Bus (USB)" refers to the "Universal Serial Bus Specification" industry specifications published by companies including Intel and Microsoft. Ex. 21, USB 1.0, at cover sheet; *See also* Ex. 22, USB 2.0, at cover sheet. The USB 1.0 (January 15, 1996) and 2.0 (April 27, 2000) specifications were released in the same timeframe as the priority utility application filing dates for the patents- in-suit. *Id.* The '624, '873, '977, '359, '768, '750, '769, and '797 patents reference USB 2.0 as the current version of the USB specification at the time. *See, e.g.*, Ex. 1, '768 patent at 12:16-18.

Like the PCI-related claims, the ACQIS USB-related claims are about compatibility and do not require every aspect of the USB specifications. Ex. 16, Levitt Decl. ¶¶ 143-144. The claims do not recite a Universal Serial *Bus* and all the aspects of the USB specifications required to implement such a bus. Instead, the inventions improve upon prior interface channels, like the Universal Serial Bus. *Id.* The claimed inventions therefore recite certain information communicated between components based on the USB specification to maintain software compatibility with existing systems while replacing the physical and electrical implementation of

the Universal Serial Bus. *Id.*

The USB-related claims at issue here recite an LVDS channel for communicating certain USB information in opposite directions. Examples include:

> a second LVDS channel coupled to the connector, adapted to convey Universal Serial Bus (USB) protocol data packets, wherein the second LVDS channel comprises two unidirectional, differential signal pairs that transmit data packets in opposite directions

Ex. 2, '750 patent at 43:28-32 (claim 24).

> a first Low Voltage Differential Signal (LVDS) channel comprising first unidirectional, differential signal pair to convey data in a first direction and second unidirectional, differential signal pair to convey data in a second, opposite direction; . . . wherein the first LVDS channel conveys Universal Serial Bus (USB) protocol through the connector to the console

Id. at 46:65-47:8 (claim 48).

> conveying a first Low Voltage Differential Signal (LVDS) channel through the connector comprising two unidirectional, serial channels that transmit data in opposite directions;
>
> conveying Universal Serial Bus (USB) protocol data from the integrated CPU and graphics controller chip, over the first LVDS channel for external USB protocol data communication

Ex. 3, '797 patent at 42:9-16 (claim 33).

> the first LVDS channel comprising two unidirectional, serial bit channels that transmit data in opposite directions; and
>
> conveying Universal Serial Bus (USB) protocol information through the first LVDS channel

Ex. 14, '140 patent at 23:15-20 (claim 18).

These claims directly contradict Defendant's position that the USB data terms require fully USB 2.0-compliant transactions including a "token packet," a "handshake packet," and a "data packet," none of which are recited in the claims. Dkt. 77 at 36. On their face, the claims do not require adherence to all aspects of the USB specifications existing at the time of the

invention. Ex. 16, Levitt Decl. ¶¶ 143-144. The prior art USB specifications addressed communication only in a single direction at a time, *i.e.*, half-duplex. *Id.* ¶ 143. The claims, in contrast, communicate USB information using LVDS channels in opposite directions, *i.e.*, full-duplex. *Id.* ¶ 144.

A POSITA would recognize that the ACQIS claims reciting LVDS channels to convey USB "data" refer to information described in the USB specifications relating to the "data payload." *Id.* ¶¶ 139-142. The USB specifications describe a "data field" to communicate data using a USB protocol. *Id.* ¶ 139; Ex. 21, USB 1.0 at § 8.4.3; Ex. 22, USB 2.0 at § 8.4.4. The USB specifications explain that "[t]he data payload is the data that is carried in the data field of a data packet within a bus transaction (as defined in Chapter 8)." Ex. 16, Levitt Decl. ¶ 139; Ex. 21, USB 1.0, at § 5.3.2; *See also* Ex. 22, USB 2.0, at § 5.3.2. By reciting USB "data," as described in the USB specifications, the claims can maintain software compatibility with USB systems while improving performance with the invention's new interface channel. *See* Ex. 16, Levitt Decl. ¶¶ 35 (describing software compatibility), 38 (describing application to USB).

The claim term "Universal Serial Bus (USB) protocol information" uses more general language than the terms addressing USB "data" and thus should have a more general meaning, covering any information described in the USB specifications. The ACQIS specifications describe "data" as a subset of "information" generally. *See, e.g.*, Ex. 1, '768 patent at 21:37-22:42 (explaining that Figures 13 and 14 show "information transmitted on the XPBus," including "data" bits and also including "address" bits, "control information," and bus status bits).

2. Defendants mischaracterize ACQIS's claim construction positions in this and other litigations.

Defendants' mischaracterize the dispute over the USB terms as an attempt by ACQIS to

cover the USB 3.0 specification, to reach beyond the disclosures of the patents-in-suit, and as conflicting with statements made in the co-pending *Samsung* litigation. However, Defendants' argument is based on cherry-picking ACQIS statements and presenting them out of context. For example, Defendants quote from Appendix F of ACQIS's Infringement Contentions Against Lenovo Defendants as follows: "Plaintiff identifies ***USB 3.0 and later*** communication channels and related hardware throughout Appendix F as satisfying the foregoing claim limitations…The ThinkSystem SR 670 has one or more **USB 3.0 or later ports**." Dkt. 77 at 34-35 (emphasis added by Defendants). Defendants use ellipses to omit a critical part of ACQIS's position:

> Plaintiff contends that any generation of USB, and any form factor of USB, satisfies "USB protocol" claim limitations literally or under the doctrine of equivalents. Every generation of USB hardware that otherwise satisfies the claim limitations below conveys USB protocol data, and differences between later-issued USB protocols and earlier protocols in this regard, if any, are insubstantial such that subsequent generations of USB are backward compatible with earlier USB version.

Defendants' Ex. 19 at 3. In other words, a communication channel can satisfy both USB 2.0 (and earlier versions) and USB 3.0 at the same time, with respect to the claim limitations. Defendants do not appear to dispute this, since they have failed to point to any differences in the USB specifications that would prevent a communication channel from satisfying more than one version of USB. Their construction would mislead the jury by explicitly stating that USB 2.0 and prior versions are within the scope of the construction and imply (incorrectly) that USB 3.0 is excluded.

Defendants point to statements made by ACQIS and its expert witness during claim construction proceedings in the *Samsung* litigation to show that ACQIS "conceded…that the claimed USB terms refer to the USB 2.0 Specification and prior versions." Dkt. 77 at 34. Defendants take these statements out of context in an attempt to argue that ACQIS previously conceded to Defendants' proposed construction, but the context is crucial. ACQIS's proposed

construction of the USB terms is identical in both litigations. *See* Ex. 29, *Samsung*, No. 2:20-cv-00295-JRG, Dkt. 65 at 26. Moreover, since Samsung and Defendants have also proposed identical constructions for the USB terms (i.e., referring to "Universal Serial Bus Specification Revision 2.0"), ACQIS is arguing against the same proposed construction in both cases. *Id.* As another example of Defendants taking ACQIS's statements out of context, Defendants relied on one sentence carefully selected from ACQIS's claim construction reply brief stating that "[T]he term 'USB' refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions" (Dkt. 77 at 34), but they ignore another sentence from the same paragraph that completely undermines Defendants' argument: "That aspects of USB 2.0 and prior versions recited in the claims also appear in later, accused versions of USB is not relevant to claim construction." Defendants' Ex. 17 at 10. ACQIS's position in *Samsung* is the same as its position in the present litigation.

ACQIS does not dispute that the claim term "USB" refers to the versions of the USB specifications (2.0 and earlier) in existence at the time of the invention. But the claims do not require every aspect of the USB specifications. ACQIS does dispute Defendants' unfounded, implicit contention that there is any meaningful difference between USB 2.0 and 3.0 that is relevant to the scope of the claim terms. The Court should reject Defendants' unsupported proposed construction for the USB terms.

3. Defendants' improperly conflate "USB protocol [data/information] with "USB protocol data packets"—a term no party has proposed for construction.

Defendants acknowledge that ACQIS proposes that "Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol data" should be construed as "USB data payload." Dkt. 77 at 32. Defendants further acknowledge that some of the patents have claims that also recite "data *packets*"—"(USB) protocol data packets" and "data packets in accordance

with a Universal Serial Bus (USB) protocol" (*id.* at 35)—but those terms were not proposed for construction by any of the parties. *See* Ex. 30, Defendants' Disclosure of Terms for Construction; Ex. 31, ACQIS's Disclosure of Terms for Construction. Nonetheless, Defendants allege, without citing any statement by ACQIS, that "ACQIS proposes that the Court construe [the data packet] terms as merely 'USB data payload'" and then devote a page and a half to argue against a strawman. Dkt. 77 at 35-36. According to Defendants, "ACQIS cannot credibly contend that a USB data packet is the same as a USB data payload" without recognizing that ACQIS *did not* take this position.[13] *Id.* at 36. Defendants also argue against ACQIS's proposed construction of "Universal Serial Bus (USB) protocol signals," which is yet another term that was not proposed for construction. As neither party proposed that these terms be construed, "data packets" and "protocol signals" are not at issue and should be given their plain and ordinary meaning.

E. "computer module"

ACQIS's Construction	**Defendants' Construction**
A computing package for providing a computing function as recited in a particular claim.	A user-removable, user-portable computer system within an enclosure comprising at least a processor, memory, and mass storage.

Defendants' proposed construction improperly reads several elements into this term while at the same time introducing unnecessary ambiguity. Specifically, Defendant's proposal to include "an enclosure comprising at least a processor, memory, and mass storage" improperly reads these elements into the "computer module" limitation. And Defendants' proposal to include "user-removable, user-portable" introduces ambiguity that is likely to confuse the jury.

[13] Defendants' conflation of "data" with "data packets" is also improper because it renders the term "packets" superfluous. *See Gen. Am. Transp.*, 93 F.3d at 770.

The Court should adopt ACQIS's proposed construction since, in contrast to Defendants' proposed construction, it is consistent with all embodiments of the invention and the express language of the different claims. Because the claims recite elements of a computer module, and those elements are not necessarily the same for each claim as shown above, ACQIS's proposed construction will aid the jury by noting that the composition of a computer module is interpreted "as recited in a particular claim."

Courts have interpreted the term "computer module" in the context of the patents-in-suit on at least two occasions. In *Appro*, Judge Davis construed "computer module" as "an assembly for providing a computing function within a computer system as recited in a particular claim." *ACQIS LLC v. Appro Int'l, Inc.*, No. 6:09-cv-148, 2010 U.S. Dist. LEXIS 77548, at *16-17 (E.D. Tex. Aug. 2, 2010). The Court there rejected the Defendants' arguments that "computer module" should be construed to include "core computing power" because the "core computing power . . . comprises the central processing unit (CPU), system memory, any auxiliary processors, and primary mass storage" and including those elements "is superfluous and confusing" in view of "specific claim limitations that recite a CPU, memory, mass storage." *Id.* at *16.

As in *Appro*, some claims of the patents-in-suit recite a processor and memory unit and their relation to the computer module. Claim 11 of the '624 patent recites "a plurality of computer modules, each computer module . . . comprising a processing unit, [and] a main memory coupled to the processing unit." Ex. 4, '624 patent 38:32-35; *see also* Ex. 5, '873 patent 43:40-44. Similarly, some of the claims of the patents-in-suit separately recite the "enclosure" limitation. Ex. 5, '873 patent 44:18-23 ("A computer module comprising: an enclosure . . . ; a processing unit . . . ; [and] a main memory). Defendants' proposed construction unnecessarily imports these elements into the computer module element. *Appro*, 2010 U.S. Dist. LEXIS 77548,

at *16-17.

Further, the patents-in-suit disclose embodiments in which the computer module does not include each of a processor, a memory, and a mass storage. For example, claim 43 of the '873 patent claims an embodiment in which the mass storage device is not contained within an enclosure of the computer module; rather the mass storage device is part of the computer system and "is shared between the computer modules." Ex. 5, '873 patent 42: 25-27; *see also* Ex. 4, '624 patent 39:14-16 (reciting the mass storage device as a component of a console that couples to a computer module rather than being a component of the computer module). This and similar embodiments would be improperly excluded if Defendants' proposed claim construction were adopted. *Eko Brands*, 946 F.3d at 1373 (refusing to adopt proposed construction that would exclude embodiments).

Defendants argue that the "user-removable" and "user-portable" limitations should be read into the term because "*many* of the alleged inventive embodiments" describe the computer module as being removable.[14] Dkt. 77 at 40 (emphasis added). By using the word "many" instead of "all," Defendants concede that the invention has embodiments in which the computer module is not user-removable or user-portable. As expressly stated by the patent specifications, the invention is not limited to portable, removable applications, but includes servers and other module computing applications:

> Merely by way of example, the present invention is applied to a modular computer environment for desktop computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or module computing applications.

[14] As explained in Section II.A, ACQIS patents cover many inventions. Some of the earlier patents and claims were directed to modular computers and blade servers that are user-removable and portable. The patents and claims at issue in this case envision a removable module in some cases, but not in all cases. The claim construction must account for all of the claims.

Ex. 1, '768 patent at 1:43-48. Once again, Defendant's proposed construction would impermissibly exclude embodiments disclosed in the specification. *Eko Brands*, 946 F.3d at 1373 (refusing to adopt proposed construction that would exclude embodiments). The fact that other related patents have claims requiring the "user-removable" and "user portable" embodiments of the invention while the claims of the patents-in-suit do not further demonstrates that these limitations should not be imported into claims where they are not recited. *See Clare v. Chrysler Grp., LLC*, 819 F.3d 1323, 1330 (Fed. Cir. 2016) (applying doctrine of claim differentiation across related patents).

In addition, "the 'user-portable' limitation introduces unnecessary ambiguity" and should not be included in the construction of computer module. *Alcatel-Lucent*, 2015 U.S. Dist. LEXIS 48339, at *21. The "user-removable" limitation suffers from the same issue. As the Court noted in *Alcatel-Lucent*, anything could be considered removable and portable depending on the user. *Id.* ("For example, whereas a driver may consider a car key to be removable from the ignition, a mechanic might consider the ignition itself to be removable."). Even if the Court finds that the computer module is necessarily "portable" and "removable," there is nothing in the specification to indicate that it must be portable and removable by a "user" as opposed to, for example, a POSITA, an IT professional, an engineer, or another technician with adequate tools and training. Defendants' proposed construction is likely to confuse or mislead the jury.

Defendants' final argument takes issue with "computing function" and "computing package" in ACQIS's proposed construction. Dkt. 77 at 41. However, Defendant does not suggest that these terms would be confusing to the jury or would otherwise not be readily understood by the trier of fact. *Id.* Judge Davis previously interpreted computer module to include "computing package" and to include "computing function." *Alcatel-Lucent*, 2015 U.S.

Dist. LEXIS 48339, at *22 ("computing package" and "computing function"); *Appro*, 2010 U.S. Dist. LEXIS 77548, at *17 ("computing function"). ACQIS's proposed construction is consistent with the intrinsic record and prior interpretations of "computer module" and should be adopted.

F. "console"

ACQIS's Construction	Defendants' Construction
A device or enclosure, housing one or more coupling sites, that connects components of a computer system.	Enclosure, housing at least one bay for receiving a computer module, which connects components of a computer system.

The '768 patent makes clear that "the console is an enclosure that is capable of housing each coupling site." Ex. 1, '768 patent, Abstract; *see also id.* at 4:31-35; 4:46-50. In addition, contrary to Defendants' assertion, the term "coupling site" is recited in claims of the patents-in-suit and adequately described therein. *E.g.,* Ex. 6, '873 patent at 43:61-65, 45:37-41 ("the enclosure is insertable into the coupling site of the console"). The specification also provides a non-limiting example in which a console includes "a chassis and a motherboard" that connects to various peripheral devices, indicating that a console can be a computing device with a motherboard, and need not be an enclosure alone. Ex. 1, '768 patent at 10:57-11:2. Thus, ACQIS's proposed construction is fully supported by the intrinsic record.

ACQIS's proposed construction recognizes that the console may be an enclosure or a device, such as a chassis and a motherboard, whereas Defendants' proposed construction excludes embodiments disclosed in the claims. *Eko Brands*, 946 F.3d at 1373. Accordingly, the Court should adopt ACQIS's proposed construction and reject Defendants' proposed construction.

G. "single chip"

ACQIS's Construction	Defendants' Construction

No construction needed. Plain and ordinary meaning.	Plain and ordinary meaning, wherein the plain and ordinary meaning is "one integrated circuit chip."

The Parties agree that the Court should adopt the plain and ordinary meaning of "single chip." Yet, Defendant proposes a definition along with their suggestion of "plain and ordinary meaning" that is not plain and ordinary meaning at all. Defendants actually propose to define single chip as "one integrated circuit chip." Dkt. 77 at 43. Defendant relies on various definitions to support its "plain and ordinary" interpretation; however, Defendant conveniently omits, from its own extrinsic evidence, definitions that do not support its preferred reading. *See, e.g., Modern Dictionary of Electronics*' definition of "chip": "1. The uncased and normally leadless form of an electronic component part, either passive or active, discrete ***or integrated***." Defendants Ex. 22 (*Modern Dictionary of Electronics', Elsevier Science & Technology* (1999) at 113) (emphasis added). Even more telling, Defendant relies upon the definition of "***integrated circuit***" with no explanation why one would interpret "single chip" to correspond with "an integrated circuit" as opposed to, for example, "a circuit" or a chip with multiple "integrated circuits." The mere fact that the adjective "integrated" is used to describe a certain type of "chip" and to separately define an "integrated circuit" shows that the plain and ordinary meaning of "single chip" is not limited to "one integrated circuit chip."

Defendant does not cite any evidence in the intrinsic record to suggest that the term "single chip" is ambiguous or otherwise requires construction. Defendants' interpretation must therefore be rejected. *Landers v. Sideways, LLC*, 142 F. App'x 462, 467 (Fed. Cir. 2005) (a claim limitation should be given its plain and ordinary meaning "unless the intrinsic evidence compels a contrary result").

H. "central processing unit"

ACQIS's Construction	Defendants' Construction
No construction needed. Plain and ordinary meaning.	Plain and ordinary meaning, wherein the plain and ordinary meaning is "a single central processing unit or core processing unit."

The Parties agree that the Court should adopt the plain and ordinary meaning of "central processing unit." Defendants here again claims to propose the plain and ordinary meaning that provides a unique definition adjusted to limit it to specific embodiments. Dkt. 77 at 44-45. Defendants' do not allege that the term is ambiguous or otherwise argue that the intrinsic record compels interpreting the term. *Id.*

Defendants rely on a single definition from the *Modern Dictionary of Electronics*, which lists the elements that central processing units contain "in general" and the functions they performs then concludes that the definition does not include or encompass multiple processing cores and therefore the components and functions "reside in a single CPU core." Dkt. 77 at 45. However, the definition also does not indicate that the components and functions that a CPU "generally" includes *must* be comprised in a "single CPU core." *See* Defendants' Ex. 22 at 107.

Further, Defendants cannot identify any mention of a "core processing unit" in the intrinsic record of any of the patents-in-suit, nor do they provide extrinsic evidence to suggest that one of skill in the art would interpret a "central processing unit" to be equated with a "core processing unit." Dkt. 77 at 44-45. Defendants proposed interpretation is divorced from the intrinsic record and is likely to confuse the finder of fact. The Court should adopt ACQIS's proposed construction.

IV. CONCLUSION

ACQIS respectfully requests that the Court adopt ACQIS's proposed constructions.

Dated: September 20, 2021

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on September 20, 2021, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the Court's CM/ECF system.

/s/ Paige Arnette Amstutz
Paige Arnette Amstutz